Docket No. 55855-DIV (71987)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	T. Ho et al.	CONF. NO.:	4010
U.S. SERIAL NO.:	10/719,912	GROUP:	2822
FILED:	November 21, 2003	EXAMINER:	K. Duong
FOR:	METHOD OF FABRICATING A THERMALLY ENHANCED WAFER-LEVEL CHIP SCALE PACKAGE		

Commissioner for Patents
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Sir:

RESPONSE TO OFFICE ACTION

Applicants are in receipt of the Office Action dated February 26, 2007 of the above-referenced application. Applicants kindly request a two-month extension of time for responding to the Office Action. Applicants respond to the Office Action as follows.

Claims 1-4 are pending in the application.

Applicants' claimed invention is directed to a method for fabricating a thermally-enhanced wafer-level chip scale package including steps of: "attaching a thermally-conductive stiffener to the back side of the semiconductor wafer," and "performing a singulation process along a straight line to cut the thermally-conductive stiffener and cut apart each chip from the semiconductor wafer" (*see* steps (4) and (5) of independent claim 1; *see also* FIGS. 4-5 and specification at page 5, line 20 to page 6, line 2).

As recited in independent claim 1, a thermally-conductive stiffener is attached to the back side of a semiconductor wafer in step (4), and ***then*** a singulation process is performed to cut apart each chip from the semiconductor wafer in step (5).

Claims 1, 3, and 4 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,392,290 to Kasem et al. ("Kasem") in view of Japanese Publication 6-349983 to Takebe, Kenichi ("Kenichi") and U.S. Patent 6,645,791 to Noquil et al. ("Noquil"). Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Kasem in view of Kenichi and Noquil, and further in view of U.S. Patent 6,403,882 to Chen et al. ("Chen"). These rejections are respectfully traversed.

Regarding the rejection of independent claim 1 over the proposed combination of Kasem in view of Kenichi and Noquil, the proposed combination does not teach or suggest a method for fabricating a thermally-enhanced wafer-level chip scale package in which a thermally-conductive stiffener is attached to the back side of a semiconductor wafer, and ***then*** a singulation process is performed to cut apart each chip from the semiconductor wafer.

Referring to FIGS. 57A-57C of Kasem, a substrate 227 is sawed at locations designated by reference number 250 "to separate it from the portions of the substrate in other chips on the wafer. The heat sink 245 is left intact" (column 10, lines 35-38 of Kasem). Subsequently, as shown in FIGS. 58A-58C of Kasem, "chip 220 is separated from other chips in the wafer by sawing through the heat sink 245" at locations designated by reference number 252 (column 10, lines 39-42).

Referring to FIG. 3A of Kasem, a backside support substrate 14 is attached to the back side of a chip 11 after a cutting operation has taken place, *i.e.,* the backside support substrates are respectively attached to the back sides of chips which have been cut from the semiconductor wafer.

In contrast, according to the Applicants' claimed invention, the thermally-conductive stiffener must be attached to the back side of the semiconductor wafer **prior to** cutting apart each chip from the semiconductor wafer.

On page 4, fourth paragraph of the Office Action of 02/26/2007, it was admitted that Kasem does not teach or suggest "performing the singulation process along a straight line such that the thermally-conductive stiffener and the semiconductor wafer are cut together."

The Kenichi reference was cited allegedly for showing such a singulation process, where reference number 10 of Kenichi was cited as allegedly corresponding to the Applicants' claimed "thermally-conductive stiffener."

According to the Applicants' claimed invention, the claimed "thermally-conductive stiffener" includes the structure and function of a stiffener, i.e., it must protect singulated chips against cracking or chipping while mounting the chips onto a circuited substrate during the flip-chip die bonding process, and against cracking or chipping during handling or transportation (see, e.g., specification at page 6, line 17 to page 7, line 3).

However, referring to paragraphs 0015 to 0017 and the English-language abstract of Kenichi, reference number 10 corresponds to a "heat-dissipating plate" or heat sink, and thus provides only a heat-dissipating function. Therefore, even if Kenichi was somehow combined with Kasem, the proposed combination would not teach or suggest the Applicants' claimed invention, at least because Kasem does not teach or suggest the use of a "heat-dissipating stiffener" as claimed.

Referring to column 5, line 59 to column 6, line 2 of Noquil, the Noquil reference merely discloses that the back surface of a semiconductor wafer can be lapped, but does not teach or suggest performing a back-side lapping process after performing a bumping process as claimed. Therefore, even if Noquil was combined with Kasem, the proposed combination would not teach or suggest "performing a back-side lapping process" after a bumping process as claimed.

For at least the reasons discussed above, the proposed combination of Kasem in view of Kenichi and Noquil does not teach or suggest the Applicants' claimed invention. Therefore, independent claim 1 and dependent claims 2-4 are patentable over proposed combination.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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